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RECENT DATA SYSTEM AND ANTENNA UPGRADES TO THE CSU-CHILL RADAR

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1 INTRODUCTION

The CSU-CHILL radar is owned and funded by the National Science Foundation and operated as a national facility by cooperative agreement with Colorado State University [Brunkow 2000]. The CSU-CHILL is a dual polarization S-Band radar with high power Klystron transmitters and dual receivers. Originally built in 1970, it has undergone frequent upgrades over the years to meet the on-going requirements of the weather research community. An example of CHILL's adaptability is a project in the summer of 2005 in cooperation with the University of Massachusetts. This research focused on the relative strength of forward- and back-scattering in the boundary layer and required the CSU-CHILL radar to be operated as a bistatic receiver while its sister radar (the Pawnee radar) was operated as a conventional transmitter/receiver. Synchronization of the two radars was facilitated by new GPS time and frequency references and new digitizer/processor systems constructed largely from off-the-shelf components. The details of the new processing system are discussed in Section 3.

2 ANTENNA UPGRADE

A major upgrade which has been on-going for several years is the design and construction of a new 8.5 meter dual-offset Gregorian geometry antenna. Dual offset antennas of this size have not been generally available, so there were a number of design issues to be resolved through a cooperative effort between CSU and the manufacturer, Vertex/RSI. The goal of the project was to produce an antenna with significantly improved sidelobe performance, while not giving up the high cross-polar performance of the current CSU-CHILL antenna.

The offset design allows a more massive feedhorn/OMT than the conventional center-fed design The new antenna has an electro-formed symmetric OMT coupled to a profiled corrugated horn (see fig. 1). The feedhorn/OMT structure can be rotated 45 degrees to allow $\pm 45^\circ$ linear polarization operation as well as the normal vertical/horizontal polarization. The port to port isolation of the OMT was measured at 60 dB. The feedhorn/OMT pattern was measured in an anechoic chamber at Vertex/RSI in the 0°, 45° and 90° planes. The peak off-axis cross-pol level was measured at -34 dB. These measured feedhorn patterns were then input into a far-field simulation software package to predict the final co- and cross- polar patterns which were used to satisfy the requirements of the critical design review.

The range testing of the new antenna was underway as of this writing, but initial testing suggests that the antenna performance is very close to that predicted by the design models. In fig. 2 the antenna is mounted on the Vertex/RSI range positioner. The surface accuracy of the main reflector was measured to be within 0.010 inches RMS. Fig. 3 shows an expanded view of main lobe in the azimuth plane for Horizontal polarization (3a) and Vertical polarization (3b). The excellent matching of the main beam patterns down to the -25 dB level achieved here is critical for Z_{DR} measurements. Note also that one of the design requirements was to 'shoulder' the first sidelobe into the main lobe for better matching between the two polarizations. The shouldering is visible at the 1.5 degree angle in fig. 3.

An example of the extended range antenna patterns is shown in fig. 4. Note the excellent close-in side-

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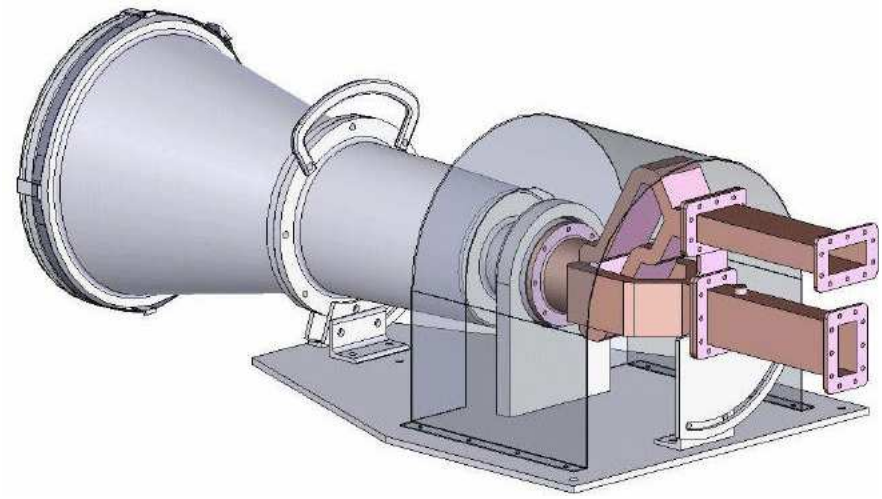


Figure 1: OMT Assembly

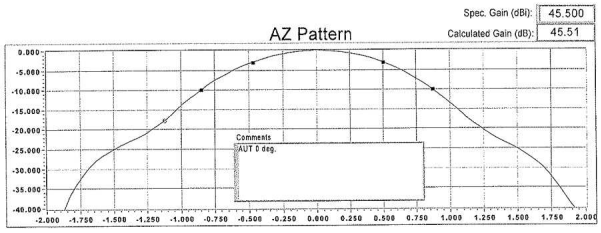
lobe performance which was similar in all the measured planes. This is only possible when the main reflector is un-obstructed as in the offset designs.

Figure 2: Offset-fed Gregorian Antenna

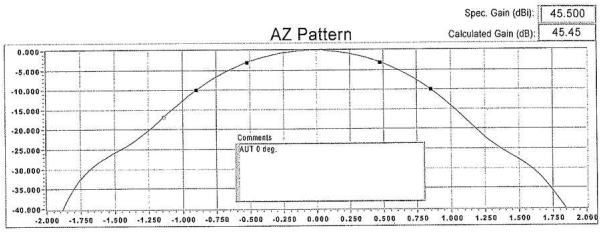
The preceding co-polar patterns were measured on the Vertex/RSI long range. The long range was not suitable for measuring low cross-pol levels because of the limitations of the polarization purity of the source antenna and also due to ground reflections. To solve this problem, Vertex/RSI built a new source horn identical to the feedhorn used on the dual-offset antenna. This source horn was mounted on the short range (228 meters) which put the source horn at a 12° elevation angle. The short range defocuses the main lobe, but the cross-polar pattern is already 'de-focused' and is considered representative of what would be measured in the far-field. All short range patterns were made by scanning the dual-offset antenna in the elevation plane from -2° to 10° which was recommended by the TDWR test report as a way to mitigate ground reflection effects.

An example of the short range co- and cross-pol patterns in the 45° plane is shown in fig. 5. Our specification called for on axis isolation of better the 43 dB and peak off-axis cross-pol in the 45° plane to not exceed -35 dB. Measurements show that this requirement was met. Note that the co-polar pattern in fig. 5 should not be interpreted as the far-field pattern. More range measurements from both the long and short range setups will be available at the time of the radar conference.

The structure to support the new dish, feedhorn, and sub-reflector is considerably larger and heavier than the current antenna, necessitating a larger radome and more powerful drive motors. Since the CSU-CHILL radar is a transportable system, the antenna structure was designed to be dismantled into 4 major pieces as shown in fig. 6. This is done in such a way that no alignment procedures are needed during reassembly.



(a) Vertical Plane



(b) Horizontal Plane

Figure 3: Radiation Pattern in Azimuth

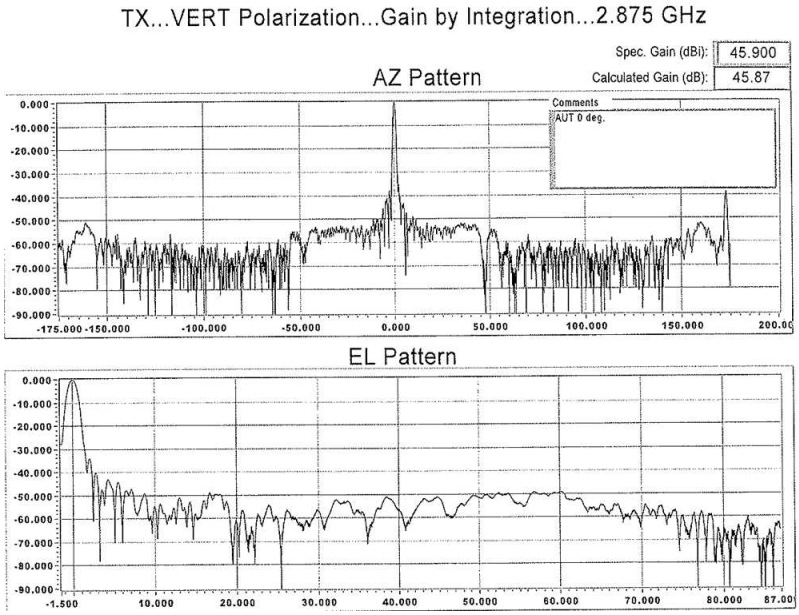


Figure 4: Azimuth/Elevation Radiation Patterns

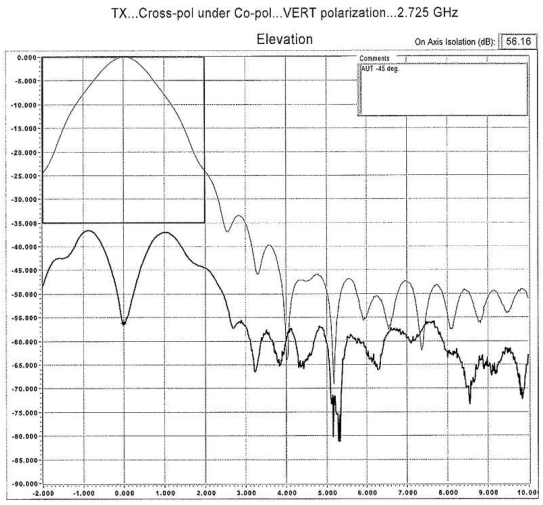


Figure 5: Close-in Radiation Pattern

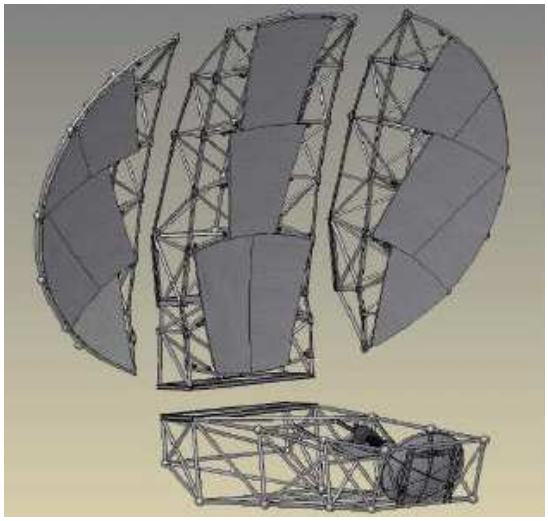


Figure 6: Reflector Sections

3 PARALLEL RECEIVER

The CSU-CHILL “Parallel Receiver” is an add-on receiver and signal processor, initially designed to operate in parallel with the existing Lassen DRX receiver and signal processor. It makes use of high-speed A/D Converters (ADCs) to directly sample the final 10 MHz IF of the receiver at a 40 MS/s rate. Signal processing such as pulse-pair processing is done using dual-CPU Intel Xeon machines running the Linux OS, interconnected by a Gigabit network. The same network can host other machines which can archive the processed data or display it in real time.

3.1 Digital Receiver Board

The CHILL Digital Receiver is based on the ICS-554 digitizer board from ICS Incorporated. This board is capable of sampling four channels at up to 105 MS/s, with a resolution of 14 bits. It makes this data available to a host computer through a 64-bit 66 MHz PCI bus. Included on the board is a Xilinx Virtex II Field Programmable Gate Array (FPGA), containing either 1 or 3 million gates, for use in post-processing the digitized data. The CSU design implements a digital down-converter, in which the final Local Oscillator (LO) is a digital 10 MHz quadrature sinusoid. Since the LO is digitally generated, the quadrature phase shift is exactly 90°, and the amplitudes are perfectly equal. The quadrature mixing is also performed digitally, eliminating I/Q gain errors which plagued analog designs.

The resulting baseband signal is filtered using a two-stage digital FIR filter. Similar commercial receiver designs make use of a simplified first stage filter, known as the Cascaded Integrator Comb (CIC), whose passband gain droop is corrected using a second filter. This requirement for droop correction complicates the design for the second stage filter, and it also reduces the available dynamic range at frequencies deviating away from zero. With this in mind, the CSU design makes use of two Finite Impulse Response (FIR) filter stages, to achieve adequate filtering down to a 1 MHz bandwidth. As a byproduct, the output of the first stage alone can be used as a 5 MS/s “oversampled” data stream. The use of two programmable FIR stages makes new filters easy to design, a useful feature in a research radar. The filter has shown good performance, achieving a rejection of 80 dB at $\pm$600 kHz, with a gain flatness of 1 dB out to $\pm$460 kHz (fig 7 and 8). This could only be achieved due to the use of an FPGA, which performs more than 3 billion integer multiplications per second when configured as a digital filter. The processing system design is shown in fig 9.

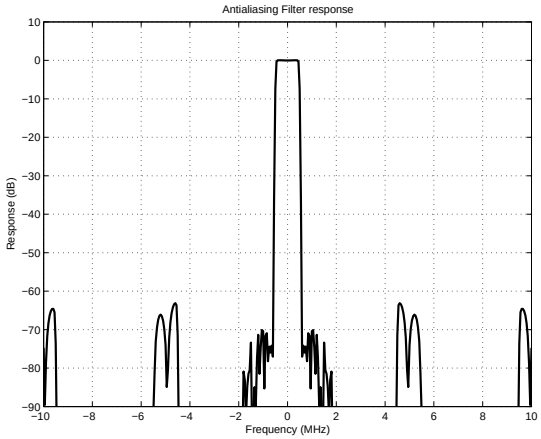


Figure 7: Anti-aliasing Filter Response

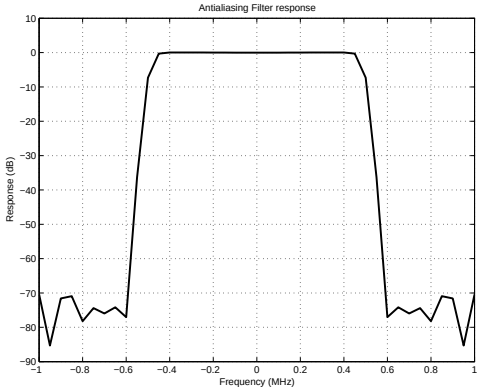


Figure 8: Close-in Frequency Response

A GPS receiver is interfaced to the receiver FPGA, which is used to append the current GPS time to the received time-series stream. The GPS unit also has a highly stable Oven-Stabilized Crystal Oscillator (OCXO), which is phase-locked to the received GPS signal from the satellites. This OCXO output (at 10 MHz) is used as the primary reference oscillator in the radar system. In this manner, two geographically separated radars can be made coherent, enabling bistatic mode of operation without the use of expensive Rubidium or Cesium timing devices.

The FPGA on the digitizer card also generates the triggers for the radar transmitter, through the use of

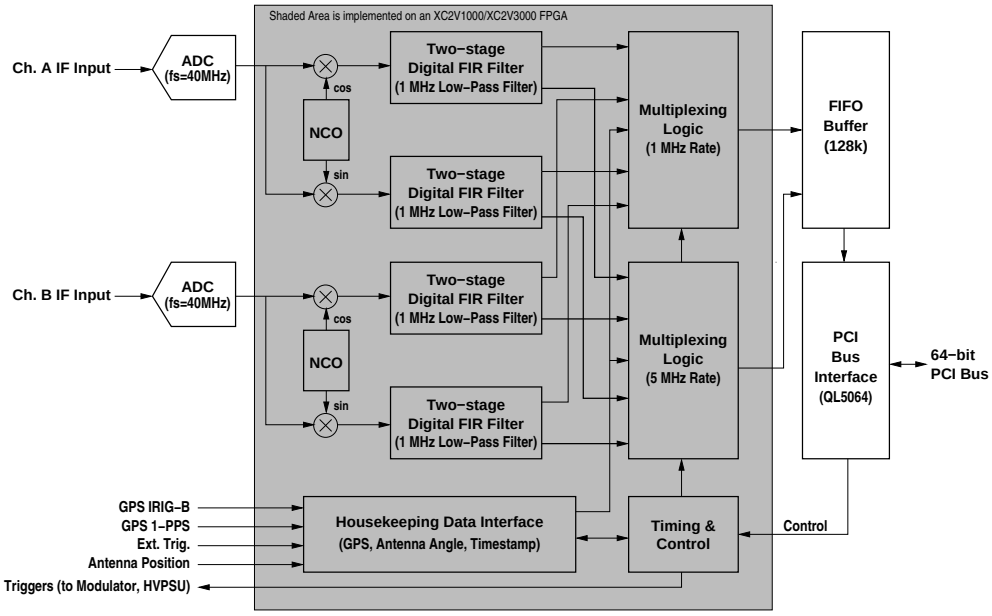


Figure 9: Digital Receiver Block Diagram

a programmable trigger generator, which can generate timing pulses to a 25 ns resolution. The timing generator can synchronize itself to the GPS receiver, ensuring that during bistatic operation, the trigger signals of the two radars are synchronized.

The FPGA-generated triggers are made available to the rest of the radar system using a custom-built board, which buffers and level-shifts the FPGA outputs. This board also serves as the GPS interface, and contains a 4 megabyte bank of fast Static RAM, which can be used by the FPGA as temporary store while performing calculations. At the moment, the digital filter does not require any additional storage, however, it may be used by new designs which use algorithms like spectral-domain processing.

The down-converted baseband data is merged with various time-critical housekeeping data, such as the current antenna position, GPS time, etc. and passed over a high-speed PCI-X bus to the acquisition host. This scheme ensures that the data and timestamps are always synchronized with each other, without the need for a hard-realtime OS running on the host computer.

3.2 Acquisition Server

The host runs an acquisition server program, which accepts the 1 MS/s and 5 MS/s streams from the digitizer board, merges it with additional housekeeping data obtained from the antenna control computer and makes it available on a TCP/IP socket. The server also implements a programmable 5-pole elliptic Doppler filter, whose output is simultaneously available along with the unfiltered data. Standard filters, with several different notch depths and rejection bandwidths are available. The acquisition server is also responsible for configuring the digitizer board and its FPGA.

The acquisition server can send the time series data out to several clients at the same time, with each client having it's own buffer memory. In this manner, network congestion affecting one client will not cause other clients to lose data. The server software is multithreaded, and can take full advantage of multi-CPU hardware.

Use of general-purpose networking hardware and protocols enables the acquisition server to provide data to remote clients, connected to the server by a high-speed network connection other than Ethernet. In this manner, time-series data can be remotely processed in real-time, using a variety of algorithms.

The server is implemented on a commodity dual-CPU Intel Xeon server, running the Linux OS. Use of open-source OS and development tools helps to keep the cost at a minimum. Interaction between various subsystems of the processing system is detailed in figure 10.

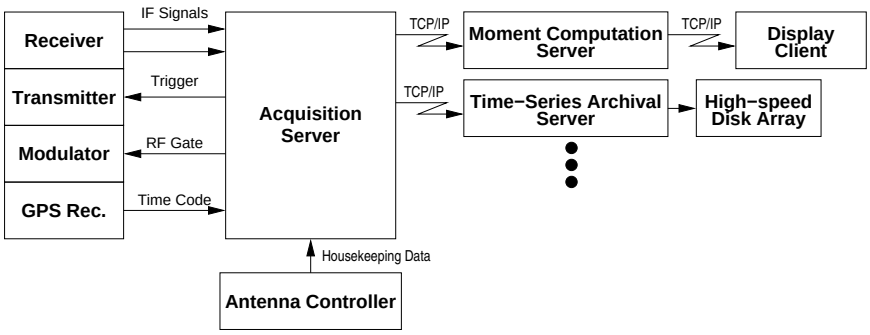


Figure 10: CHILL Receiver Block Diagram

3.3 Client Programs

Client programs (data sinks) can connect to the acquisition server and request time series data, along with the housekeeping and status information. Several clients can connect to the server at the same time, limited only by the network and memory bandwidth available to the host computer. Several client programs are available, including data visualization programs, time-series archival, moment data calculation and archival, status displays, etc. Since the protocol used for network communications is TCP/IP, clients can be written for any platform which supports TCP/IP. The clients developed so far are for the Linux OS.

4 CONCLUSION

The antenna upgrade to CSU-CHILL will improve it's sidelobe rejection capability, by eliminating strut blockage effects, while retaining the cross-polar performance of the existing antenna. The receiver/signal processor upgrade improves CHILL's ability to support the research community by virtue of it's highly programmable and open nature, and it's ability to provide and record large quantities of time-series data. The GPS-synchronization capability has already found use in the recently concluded bistatic-mode operations, and will enable further research into bistatic reflections from precipitation.

Acknowledgments

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References

[Brunkow 2000] David Brunkow, V. N. Bringi, Patrick C. Kennedy, Steven A. Rutledge, V. Chandrasekar, E. A. Mueller, and Robert K. Bowie, 2000: **A Description of the CSU-CHILL National Radar Facility**. *Journal of Atmospheric and Oceanic Technology*, Vol 17, No 12, pp 1596-1608.