8B.3 A GENERIC RADAR PROCESSOR DESIGN USINGSOFTWARE DEFINED RADIO

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1. INTRODUCTION

Signal processors for research weather radars have been conventionally designed and built using custom electronics to fit the needs of individual radar platforms. With the increasing need to develop new radar platforms while upgrading and maintaining those of which are still used by the scientific community, the time and money resources needed to continue this conventional method of design can easily outweigh that of which is available. In order to minimize these resources, there is a need to develop a generic radar signal processor that is compatible across multiple radar platforms. Field Programmable Gate Arrays (FPGAs) provide a suitable technology for this purpose. By judiciously choosing the processing architecture implemented within the FPGA, a wide range of radar intermediate frequencies (IFs), gate spacings, and signal bandwidths can be accommodated using the same design. This paper assumes a design method in which the output data bandwidth is inversely proportional to the radar transmit pulse width.

There are many commercially available software defined radio (SDR) boards that can meet the needs of the generic radar signal processing application. These boards provide high speed analog to digital converters (ADCs) capable of digitizing a wide array of IFs, and FPGAs capable of implementing the signal processing algorithms of generic digital down converters. These generic digital down converters are made up of real-time programmable components such as filters, oscillators, and decimators that are capable of adapting to fit the needs of multiple radar platforms. Post processing algorithms such as spectral and pulse pair processing can also be implemented directly within the FPGA in order to eliminate the need for separate hardware and meet bus bandwidth limitations. These SDR boards are compatible with standard rack mount PCs which do not require specialized buses or operating systems. A block diagram of a typical 4 channel SDR board is shown in Figure 1.

This paper will discuss an architecture that can be implemented using commercially available SDR boards to meet the needs of multiple radar platforms. Section 2 presents the digital down conversion process implemented by a generic radar processor, and the demodulation schemes and filtering techniques used to cover a wide array of input signal bandwidths. Section 3 presents the system performance obtained with the new

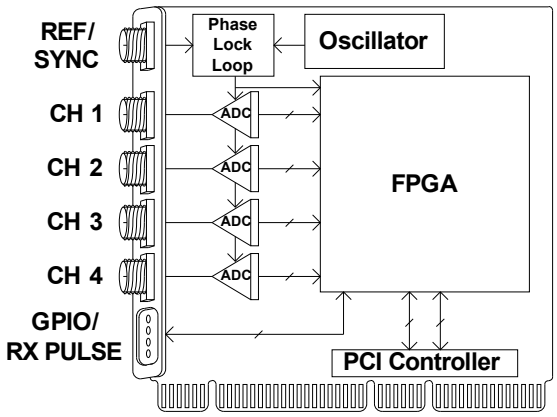

Figure 1 - Typical block diagram of a commercially available four channel SDR board.

SDR radar processor board for the X-band ELDORA dual-beam airborne Doppler radar. Section 4 discusses the post processing of IQ samples and the ability to do so within the FPGA as has been done with the new ELDORA radar processor in order to maintain the functionality of the original RP7 radar processor, (Hildebrand et. al. 1996).

2. DIGITAL DOWN CONVERSION

A block diagram of the generic digital down conversion process is shown in Figure 2.

The digital down conversion process begins with the digitization of the IF input. Many SDR boards are available with high speed ADCs like the LTC2255, by Linear Technology, which is capable of obtaining 14 bit resolution and 72 dB of signal to noise ratio (SNR) at speeds up to 125 MSPS. At this sampling speed, IF frequencies up to 62.5 MHz can be sampled at or above the Nyquist frequency while IF frequencies greater than 62.5 MHz can be still be supported using undersampling techniques, (McCormack 2004).

After the IF is digitized by the ADC, the samples are digitally down converted by the FPGA by splitting the data into separate complex, in-phase (I) and quadrature phase (Q), data channels and digitally mixing these data channels with the sine and cosine outputs of a numerically controlled oscillator (NCO). This process is done using a digital mixer, consisting of a digitally tunable NCO, along with simple multipliers which can be implemented within the FPGA in order to

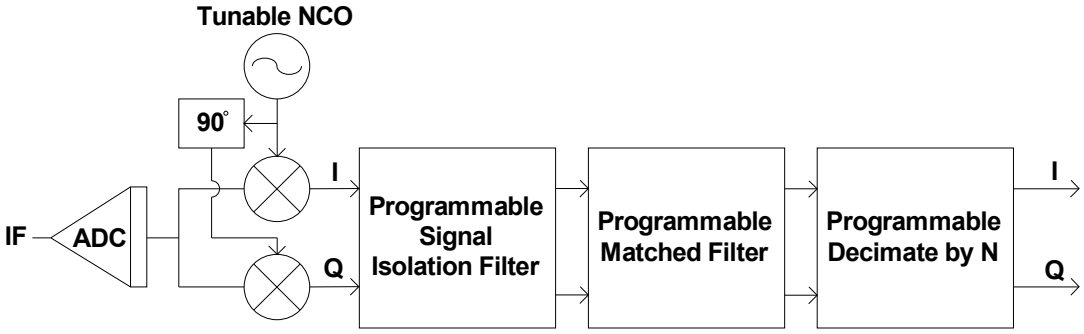

Figure 2 - Generic Digital Down Converter.

produce both I and Q data at DC, (Paul et al. 2007, Hosking 2006). This NCO is implemented using the Xilinx DDS v5.0 IP and is tunable over its frequency range from DC to half of its sampling frequency and can achieve a frequency resolution of 0.02 Hz and a spurious free dynamic range (SFDR) of 115 dB using a 100 MHz sampling clock source, (Paul et al. 2007, Hosking 2006), Thus, the use of this tunable NCO, allows any IF input, within the limitations of the NCO's frequency resolution, to be mixed down to DC. The digital mixer in Figure 2 consists of the NCO, phase shifter, and two multipliers which result in both I and Q data channels.

After the signal of interest is split into I and Q channels and mixed down to DC, two first stage filters are used to isolate the signal of interest from the sum frequency image created during the mixing process as well as decimate the data rate to allow for a more efficient second stage matched filters. Efficiency is the goal for filter design and a polyphase decimating finite impulse response (FIR) filter is an efficient filter architecture in which the data rate can be decimated prior to filtering. This drastically reduces the number of multiplication operations needed to produce each output sample, (George 2006, Hazanchuk & Lim 2003). To improve the hardware resource efficiency even further, filter symmetry can be used in order to cut the number of needed multipliers in half. By exploiting the fact that a symmetric filter contains all matching filter coefficients, the corresponding data need only be added and then multiplied once, (Andraka & Berkun 1999, Hazanchuk & Lim 2003). This filter architecture can be implemented to decimate the data rate by any factor of 4 that best matches the maximum needed output rate, i.e. 4, 8, 12, etc. In order to achieve the desired filter characteristics of a flat pass band, sharp transition band, and good stop band attenuation, a Kaiser Window function can be used, (George 2006). This filter architecture using even symmetry and even filter order is shown in Figure 3.

If the required resources for the two first stage filters and digital mixer are too much, another method can be used in which IF flexibility is traded to save FPGA resources. By carefully choosing the sampling frequency to be 4 times greater than the IF frequency, a single first stage digital filter can be used to convert the incoming IF data stream into complex, I and Q, data at DC, (George 2006, Mitchell 1989, Rader 1984). Under these conditions, the NCO output is reduced to a series of 1s, 0s, and -1s therefore eliminating the need for multipliers, and making it possible to incorporate the mixing process into the first digital filter stage, (Andraka & Berkun 1999, George 2006). If this method is used, the entire digital mixer and first stage digital filtering, consisting of the NCO, two multipliers, and two digital filters, can be realized using a single first stage digital filter. This filter architecture using even symmetry and odd filter order is shown in Figure 4.

After the maximum desired signal bandwidth is isolated by the first stage filtering, the second stage filtering consists of two matched filters used to detect the presence of severely attenuated weather echoes. There are many matched filter functions that can be chosen to best fit the application, such as a Gaussian function which is used to maximize SNR, (Doviak & Zrnic 1993). With the data rate already decimated from the first stage filtering, each second stage filter is realizable as a single rate filter. Filter symmetry can also be exploited with the second stage filters. This filter architecture using even symmetry and even filter order is shown in Figure 5. In order to make both, first stage and second stage, filters generically adaptable to different radar pulse widths, the filter coefficients must be programmable. User defined filter coefficients can easily be read from file and programmed in real-time using FPGA RAM resources.

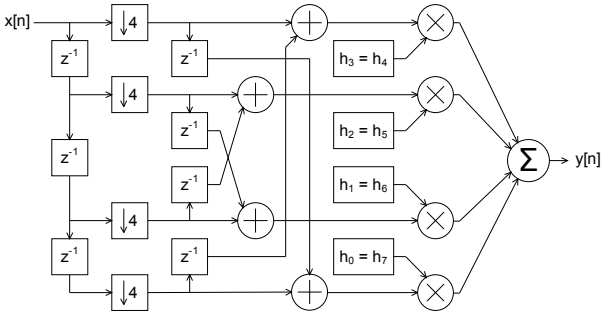

Figure 3 - Polyphase Decimating FIR Filter Architecture with symmetry.

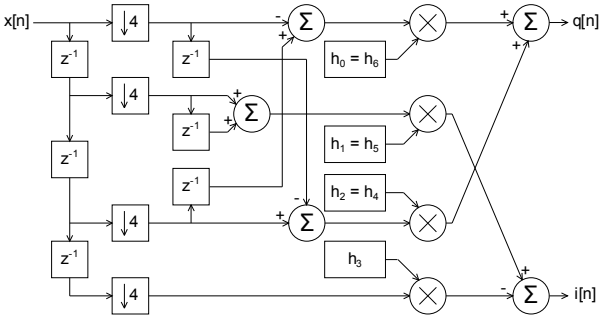

Figure 4 - Polyphase Decimating FIR Filter Architecture with symmetry for 4 times sampling frequency method.

After the data has been processed by both filter stages, the last step is to decimate the data down to the rate which matches the transmit pulse width of the radar. By implementing a programmable decimator within the FPGA, any data rate could be achieved to correspond to any pulse width. A programmable data decimator is easily implemented within the FPGA by using a programmable clock divider to register the data from the output of the second stage filter.

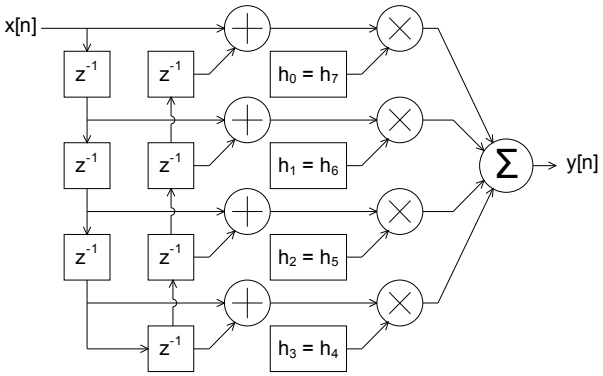

Figure 5 - Single Rate FIR Filter Architecture with symmetry.

3. DEMONSTRATED PERFORMANCE

The performance of the SDR based processor boards was investigated by computing the signal to noise ratio, synonymous with effective dynamic range, achieved under typical operating conditions. Many high speed ADCs are capable of producing digital samples with more than 70 dB of SNR. However, a radar signal processor is not limited to the SNR of the ADC. Process gain is achieved by the filtering and downsampling that takes place within the digital down converter as well as any oversampling that takes place within the radar processor, (Kester 2005). Process Gain is given by

$$\text{Process Gain} = 10 * \log_{10} (fs / (2 * BW)) \quad (1)$$

where fs is the sampling frequency of the ADC and BW is the filtered bandwidth of the signal of interest. An extra 20 dB of process gain can be realized by effectively filtering with a pass band filter bandwidth of 500 kHz while the ADC samples at a rate of 100 MHz.

The new ELDORA radar processor consists of 2 Channel Adapter M314 cards, manufactured by Red Rapids, each of which uses four LTC2255 ADCs and a single FPGA to process 4 parallel independent IF channels. Data from the new ELDORA signal processor was analyzed to show the effects of process gain on the radar processor. As Figure 4 shows, 85 dB of SNR was achieved using an ADC that provided 71 dB of SNR and process gain that provided 14 dB of SNR. The measured SNR of the new ELDORA radar processor, shown in Figure 6, exceeds the typical weather radar requirement, which is on the order of 80 dB. This data was taken by undersampling a 60 MHz IF at a sampling frequency of 48 MSPS using a bandwidth of 1 MHz. To best interpret Figure 6, 27 dB of FFT gain was introduced by the 1024 Point FFT computation.

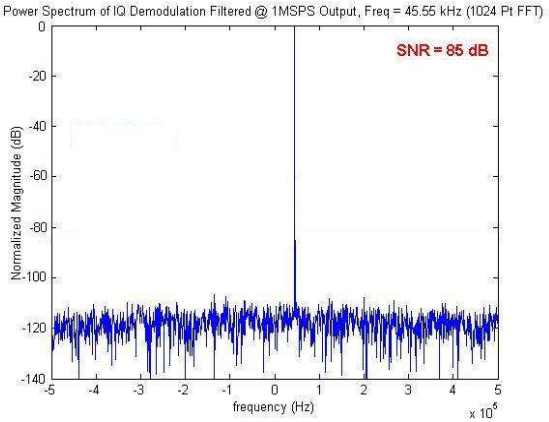

Figure 6 - New ELDORA Signal Processor SNR Plot

4. POST PROCESSING DATA

The streaming IQ data that is output from digital down converter must be further processed in order to retrieve the radar reflectivity, velocity, and spectral width estimates. There are two post processing techniques that can be used to obtain the needed information for these estimates; pulse pair and spectral processing, (Doviak & Zrnic 1993). Due to advancement in commercially available PCs, both processing techniques can be implemented using high level software algorithms as opposed to the traditional hand optimized assembly code running on specialized hardware. These general purpose PCs are capable of accepting streaming IQ data directly from the digital down converter card and possess enough power to process this data at speeds compatible with most weather radar systems. Spectral processing can be achieved using Fast Fourier Transform algorithms that are freely available, such as the Fastest Fourier Transform in the West (FFTW), (Frigo 1999).

With the advancement of the FPGA, separate hardware is no longer needed to implement either pulse

pair or spectral processing as they can be implemented within the FPGA itself, (Andraka & Berkun 1999). In many multiple channel radar systems this is required where there is insufficient bus bandwidth to handle the complete time series data. This was such the case with ELDORA which requires processing for 8 parallel channels using a single PCI bus. Pulse pair engines were implemented within the FPGAs to produce both power and velocity vector data at a much lower data rate. Because pulse pair processing requires sufficiently fewer hardware resources it is still the more attractive technique used in FPGA hardware. However, FFT engines are easily implemented within an FPGA to provide the needed framework for spectral processing.

5. CONCLUSION/FUTURE WORK

By using the provided architecture, a single radar signal processor with multiple parallel channels of efficient digital down converters can be implemented within a single FPGA and be generic enough to adapt to the needs of multiple radar platforms. Post processing techniques, such as pulse pair processing, can also be implemented within the FPGA to meet bus speed requirements.

The generic design described within this paper has been implemented and used for the next generation of the ELDORA radar signal processor. This new radar signal processor contains programmable filters and decimator that allow it to adapt to the many different pulse widths that ELDORA uses. Once the new ELDORA radar processor is integrated into the ELDORA radar, the range gate capabilities will increase from roughly 400 gates to 1000 gates and the SNR will increase from 70 dB up to 85 dB.

After the completion of the integration of the new ELDORA radar processor, the benefits of this design architecture will be leveraged as work begins on the radar processor for the Hiaper Cloud Radar (HCR), (Farquharson et al. 2007). Much of the new ELDORA radar processor design will be easily implemented within the HCR radar processor thus minimizing the design efforts. There are other conceptual radar platforms, such as the Community Airborne Platform Remote-Sensing Interdisciplinary Suite (CAPRIS), (Loew et al. 2007, Moore et al. 2007), that would especially benefit from a generic radar signal processor as multiple radars would coexist within a single airborne platform. In such a case as CAPRIS, overall design efforts would be drastically reduced if each radar instrument was capable of using the same generic radar processor design.

6. REFERENCES

Andraka, R. and Berkun, A., 1999: FPGAs Make a Radar Signal Processor on a Chip a Reality. *Conference Record of the Thirty-Third Asilomar Conference on Signals, Systems, and Computers,* Pacific Grove, CA, IEEE, 559-563.

Doviak, R. J. and Zrnic, D. S., 1993: Doppler Radar and Weather Observations, 2nd ed. Academic Press, San Diego, CA.

Farquharson, G. and Coauthors, 2007: A New High-Altitude Airborne Millimeter-Wave Radar for Atmospheric Research. *33rd International Conference on Radar Meteorology,* submitted.

Frigo, M., 1999: A Fast Fourier Transform Compiler. Proceedings of the ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 169-180.

George, J., 2006: Parallel Receiver Characterization Report. *Private Communication*.

Hazanchuk, A. and Lim, S. Y., 2003: Optimizing Up/Down Conversion with FPGA Techniques. Retrieved 10 August, 2005, from http://www.commsdesign.com/

Hildebrand, P. H. and Coauthors, 1996: The ELDORA/ASTRAIA Airborne Doppler Weather Radar: High-Resolution Observations from TOGA COARE. *Bull. Amer. Meteor. Soc.*, 77, 213-232.

Hosking, R. H., 2006: Digital Receiver Handbook: Basics of Software Radio, 6th ed. Retrieved 30 May, 2007, from http://www.pentek.com/

Kester, W., 2005: Taking the Mystery out of the Infamous Formula, "SNR=6.02N+1.76dB," and Why You Should Care. Retrieved 20 February, 2007, from http://www.analog.com

Loew, E. and Coauthors, 2007: An Airborne Phased Array Radar Concept for Atmospheric Research. *33rd International Conference on Radar Meteorology*, submitted.

McCormack, P., 2004: Effects and Benefits of Undersampling in High Speed ADC Applications. Retrieved 30 May, 2007, from http://www.national.com/appinfo/adc/files/Undersampling.pdf

Mitchell, R. L., 1989: Creating Complex Signal Samples from a Band-Limited Real Signal. *IEEE Transactions on Aerospace and Electronic Systems,* **25**, 425-427.

Moore, J. and Coauthors, 2007: Development of Advanced Radar and Lidar Platform Suite for Interdisciplinary Airborne and Ground-Based Remote-Sensing Research. *33rd International Conference on Radar Meteorology*, submitted.

Paul, S., Khatri, S. P., Martin, C., Brimeyer, T., Loew, E., and Vivekanandan, J., 2007: FPGA Based Signal Processing Platform for Weather Radar. *International Geoscience and Remote Sensing Symposium*, submitted.

Rader, C. M., 1984: A Simple Method for Sampling In-Phase and Quadrature Components. *IEEE Transactions on Aerospace and Electronic Systems*, **20**, 821-824.