AN UPDATE ON MULTI-CHANNEL RECEIVER DEVELOPMENT FOR THE REALIZATION MULTI-MISSION CAPABILITIES AT THE NATIONAL WEATHER RADAR TESTBED

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Abstract

This paper describes the status of a new project that will digitize radar signals coming from eight channels on the phased array antenna at the National Weather Radar Testbed (NWRT) in Norman, Oklahoma. At the current time, a single-channel digital receiver is operational to mimic the current WSR-88D capability. The multi-channel digital data will foster a new generation of adaptive/fast scanning techniques and space-antenna/interferometry measurements, which will then be used for improved weather forecasting via data assimilation. Differing from the conventional rotating radar, the phased array is suited for multi-mission capabilities so that a variety of targets may be observed simultaneously with a high degree of fidelity. The development of a multi-channel receiver will be the catalyst and an enabling tool for research in this area for the next decade. This collaborative project, which involves scientists and engineers from the University of Oklahoma and the National Severe Storms Laboratory in Norman, is the result of a recently funded a grant from the National Science Foundation (as described in the Acknowledgement section of this paper).

Instrumentation of the phased array radar system with a multi-channel receiver suite will bring the full creativity of researchers using advanced techniques for maximizing the information from radar observations, and optimally using them in numerical models to improve weather prediction. The multi-channel receiver will collect signals from the sum, azimuth-difference, elevation-difference, and five broad-beamed auxiliary channels. One of the major advantages of the NWRT is the capability to adaptively scan weather phenomena at higher temporal resolution than is possible by the WSR-88D. Hemispherical coverage in 1 min or less vs. 4 min, can be accomplished without comprising data accuracy. The multi-channel receiver will allow direct implementation of inteferometry techniques to measure cross-beam wind, shear and turbulence within a radar resolution volume. Access to the auxiliary channels will enable clutter mitigation and advanced array processing for high data quality with short dwell times. Potential benefits of high quality and high resolution data together with cross-beam wind, shear and turbulence include better understanding of storm dynamics and convective initiation, better detection of small-scale phenomena including tornado and microburst, ultimately leading to increased lead time for warnings, and improved weather prediction.

1. INTRODUCTION AND MOTIVATING FACTORS

This paper is the second in a series that describes a project that will digitize radar signals coming from eight channels on the phased array antenna at the National Weather Radar Testbed (NWRT) in Norman, Oklahoma, see also [Yeary et al., 2008]. The current configuration of the single-channel digital receiver is designed to mimic the current WSR-88D capability. The full power of adaptive sensing, resolution enhancement, quality improvement, and measuring new meteorological parameters can be explored by developing a suite of digital receivers to access signals from existing multiple channels on the antenna that are not yet instrumented. The impact of the additional crossbeam wind/shear/turbulence measurements, and the higher data rates, achieved through adaptive and optimal scans, and their improved data quality on three-dimensional retrieval of the wind, thermodynamic and microphysical state of the atmosphere will be systematically evaluated within several existing and future projects. Figure 1 summarizes all the research components and their feedback into the receiver design and operation.

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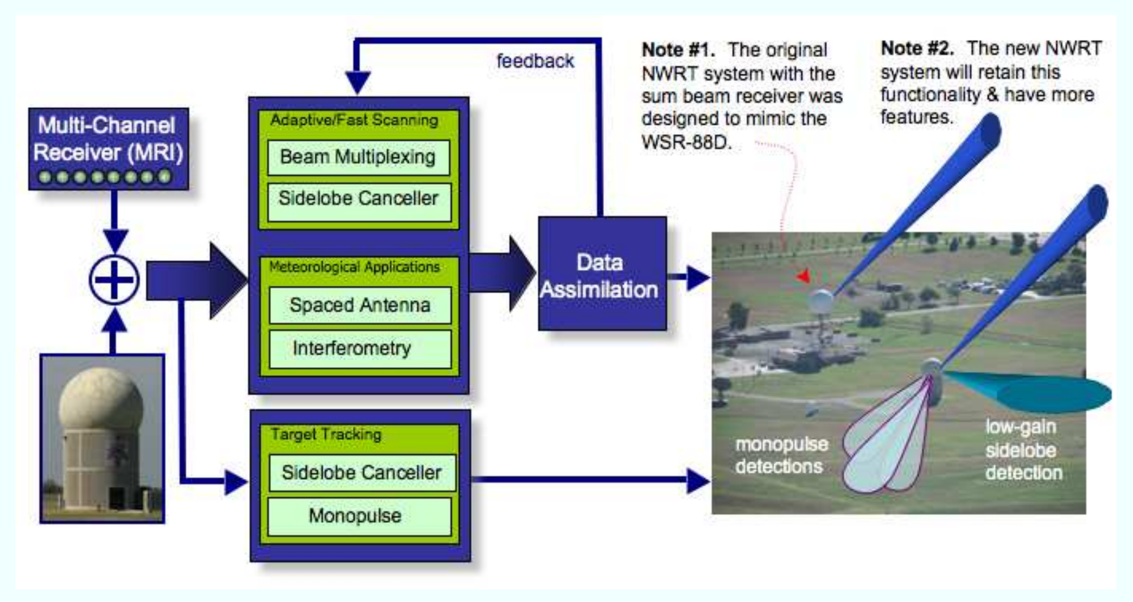

Figure 1: *The current National Weather Radar Testbed plus the proposed multi-channel receiver yields a system that supports multi-mission capabilities.*

A digital receiver suite is being built which will enable researchers using the National Weather Radar Testbed (NWRT) access to all the functionalities normally found on multi-function radars. This receiver suite will replace the current single channel (sum-beam) receiver system with an eight-channel suite to receive, digitize and record sum, azimuth difference, elevation difference and a combination of five auxiliary channels. All of these channels are available with no modification to the SPY-1 Phased Array antenna at the site. The receiver suite will be made “drop-in” compatible with the current antenna and processor system. The OU team will continue to work closely with the National Severe Storms Lab to assure the design can interface with the current system, and the operation of the integrated system will include all the functionality of the current system in addition to the multi-function hardware made possible by this MRI development. Details about the current system can be found in [Forsyth et al., 2008]. As in the current system, access to the multi-mode functionality will be available for remote operation from the National Weather Center operations center. The addition of the multi-channel receiver system will allow the NWRT to be configured as a multi-function radar, which is consistant with national needs, [NRC, 2002; JAG/PARP, 2006; NRC, 2008; Zrnic et al., 2007; Weber et al., 2007; Benner et al., 2007]. Key areas of scientific research on the completed project will be oriented around:

- Beam Multi-Plexing (BMX) – Rapid scanning is one of the primary motivating factors. A phased array radar can directly collect statistically independent samples by revisiting the region of interest through flexible beam steering to optimize the data quality [Yu et al., 2007]. Applications include tornadic observations and storm tracking.

- Generalized Sidelobe Canceller – The next motivating factor is the ability to implement spatial filtering, which is not possible with the conventional WSR-88D. Clutter filtering using signals from sidelobe cancellers (SLC) becomes essential to optimize radar performance [Le et al., 2009]. Applications include BMX and refractivity measurements [Cheong et al., 2008].

- Spaced Antenna Interferometry – The motivation for this application is to estimate crossbeam wind, shear, turbulence, and to resolve discrete targets and reflectivity inhomogeneities within the radar’s resolution volume [Zhang and Doviak, 2007, 2008]. There is potential to improve forecasts and quantitative precipitation estimates based upon the assimilation of high resolution data. Cross-beam Wind Measurements: another motivation is to acheive spaced antenna interferometry to estimate crossbeam wind, shear and turbulence . The vector wind, shear and turbulence are needed to fully understand, quantify and forecast weather.

- Data Assimilation – The final motivating factor is the ability to improve the existing data assimilation techniques by offering new state variables to gain a fuller description of the state of the atmosphere and to initialize numerical weather prediction (NWP) models [Xue et al., 2003].

2. MULTICHANNEL RECEIVER

The SPY-1A antenna array was designed to provide robust monopulse and sidelobe cancellation capabilities. The functionality is facilitated by existing azimuth and elevation difference channels and additional sidelobe channels in addition to the primary sum channel. Currently only the sum channel is instrumented in the NWRT. Utility of the additional channels has received much attention among researchers. The difference channels, for example, can be used to estimate transverse wind fields and sidelobe channels can be useful in reducing obscuration of weather by stationary targets. The multi-channel receiver features 8 high-speed digital receivers to acquire and process eight signals simultaneously from the antenna array in real-time. Figure 2 in [Yeary et al., 2008] shows a simplified block diagram of the system. RF signals from the low-noise amplifiers (LNAs) that are mounted on the array will be supplied to the analog receiver subassembly. After filtering and down-conversion the analog receivers provide intermediate frequency (IF) signals to the digital receiver chassis which produces the digital time-series data suitable for ingest by processing and recording engines.

A critical component in development of the multi-channel receiver system that makes use of all ports available on the NWRT antenna is a computer-controlled, waveguide switch that can manage the distribution of the antenna sum beam signal between these receivers. The desired modes include switching the main beam signal between the in-place receiver and a new, sum-beam, receiver in a multi-channel receiver suite (diplex mode); or allowing the sum-beam return from the antenna to be shared between these two receivers: each receiver getting 50% (duplexed mode) of the energy from each radar return signal. The new receiver estimates of the target azimuth and elevation angles depend on phase and amplitude comparisons of the sum return to two other, identical path-length antenna ports known as the elevation azimuth and elevation difference ports.

2.1. Analog Receiver Subassembly

The RF signals from the antenna are initially amplified by LNA devices that are mounted on the back side of the array. The outputs from these amplifiers are introduced to the analog receiver subsystem for filtering and down-conversion. For each channel, coherent conversion to IF is accomplished by two mixer stages using two local oscillator signals from the existing exciter chassis. In addition, a coherent reference signal and a trigger pulse from the existing real-time controller (RTC) are buffered and conditioned for the digital receiver modules. The first mixer stage converts the 3200 MHz input signal to 750 MHz using a 3950 MHz local oscillator signal (LO1) from the exciter. The bandpass filter selects the lower sideband at 750 MHz and attenuates the remaining mixer artifacts. The second mixer converts the 750 MHz signal to 50 MHz using a 700 MHz local oscillator signal (LO2) supplied by the exciter. Another bandpass filtering stage is needed to pass only the lower sideband. The resulting IF signals are buffered and supplied to the digital receiver chassis for processing. The digital receivers also require a coherent reference clock and a trigger pulse for synchronization. These two signals are available from the exciter and the real-time controller (RTC). They are split and conditioned for the next stage. Since the configuration is based on four 2-channel digital receiver modules, four copies of the clock signal and trigger pulses are produced for the digital receivers.

2.2. Digital Receiver Subassembly

The digital receiver chassis contains all of the equipment necessary to ingest the eight analog IF signals and produce a multi-channel digital data stream suitable for processing and/or recording by user equipment. The digital receiver modules convert the IF signals to discrete samples using 14-bit analog to digital converters (ADCs). Although these converters are capable of sampling in excess of 100 MHz, they are clocked at 80 MHz. Raw discrete samples are converted to in-phase and quadrature (I & Q) components and then filtered by programmable filtering stages. The resulting high data rates are not suitable for many conventional buses. Therefore, a very high-speed serial transport fabric will be used to reliably transfer all data to their required destinations.

The output data from the digital receivers must be encapsulated and tagged with acquisition parameters to clearly identify each radar pulse. Thus all data from the digital receivers are dumped into bulk memory where they are encapsulated and tagged by the host computer prior to transfer to external user ports. Acquisition parameters are extracted by the RTC from user-supplied stimulus (STIM) files which control the overall operation of the radar system. The host computer in the digital receiver chassis can obtain this information directly from the RTC or the original STIM files using the local area

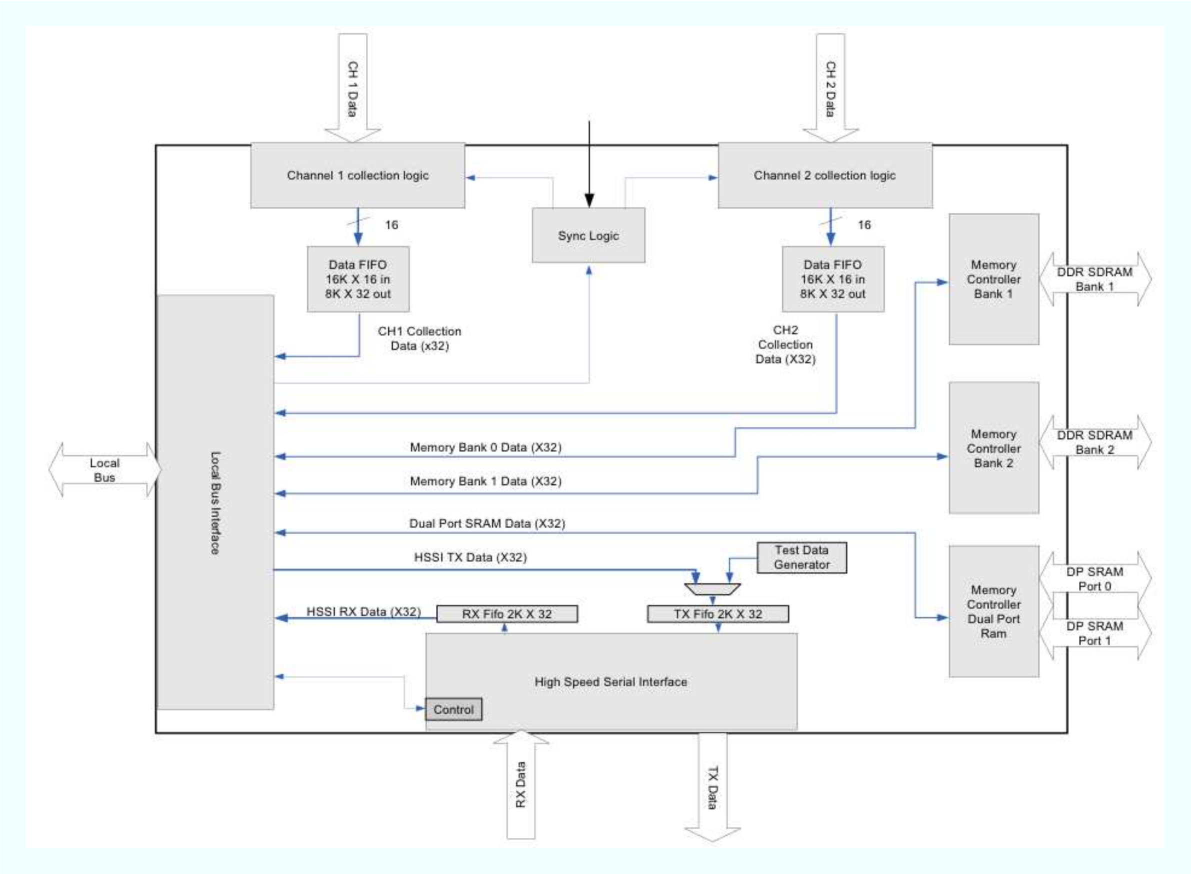

Figure 2: *FPGA based PCIX block diagram for high-bandwidth data transfer. The PCIX provides the primary interface between the eight digital receivers and the host computer. The PCIX interface is implemented in a Xilinx XCV4LX25 FPGA and utilizes the Xilinx PCI-X core for the interface.*

network (LAN). Trigger pulses synchronize operation of the digital receivers and facilitate encapsulation of the data.

In order to reliably transfer large amount of data to user equipment special input/output modules are required. These devices have special embedded processors and have access to the bulk memory through the transport fabric. Upon command from the host computer the direct memory access (DMA) controllers on these modules transfer data pulse by pulse from memory to user equipment.

To implement the digital receiver assembly, an Echotek receiver system from Mercury will be implemented in the next few months. The EchotekTM Series ECV4-2 family of wideband digital receivers from Mercury Computer Systems implements a flexible field-programmable gate array (FPGA) based architecture in a space-efficient PMC/XMC form factor. The flexibility and power of the VirtexTM-4 FPGAs allow the family to deliver unique capabilities, such as multi-board coherency, while addressing a range of analog signal requirements.

Figure 2 depicts the interface to the host computer. The PCIX FPGA provides the primary interface between the ECV4-2-2R130-1T500-XMC board and the host computer system. The PCIX interface is implemented in a Xilinx XCV4LX25 FPGA and utilizes the Xilinx PCI-X core for the interface. The PCIX FPGA contains a Xilinx LogiCore PCI-X Version 5.0 core in a XCV4LX25 FPGA. This core supports PCIX 133MHz, 100MHz 66MHz and PCI 33MHz. The control path interface of the FPGA contains the logic for the local control bus and the flash programming interface. The data path interface of the FPGA contains the logic for the high speed data transfer path. This block is used to move data between the User FPGA and the PCIX Bus. The path consists of the following blocks: 1) PCI Master logic. 2) High Speed Serial Transmitter logic, FIFOs and control. 3) High Speed Serial Receiver logic, FIFOs and control. 4) Auto DMA Logic. In normal mode, a DMA descriptor is associated with a single data buffer in system memory. When the DMA is initiated the specified amount of data is moved to/from the data buffer. Upon completion of the DMA, the DMA engine either advances to the next DMA descriptor or halts based on the End of Chain field. In auto-increment mode, a DMA descriptor is associated with multiple contiguous data buffers in system memory. Each data buffer must be of the same size. The descriptor contains a Number Buffers field. Upon completion, the DMA moves the same amount of data to/from the next contiguous data buffer. This is repeated until the last data buffer has been used. At this point, the DMA engine either advances to the next DMA descriptor or halts based on the End of Chain field.

The ECV4-2 is designed to support a broad range of digital receiver applications. The receiver channel synchronization allows all important receiver functions to be synchronized across all receiver channels in a multi-board configuration using front-panel sync input and sync output connectors. This capability makes the ECV4-2 especially well-suited for beamforming and direction-finding as required by radar, SIGINT, ELINT, medical imaging, and communications. The ECV4-2 product family supports two FPGAs. One Xilinx Virtex- 4 FX, SX, or LX FPGA functions as the primary data processor. This FPGA allows the user to run custom algorithms such as digital down/up conversion (wideband or narrow-band), fast Fourier transforms (FFT), and filtering directly on the board. The default board verification IP will be available from Mercury to implement its own IP, and the verification IP includes the basic functionality required to verify the operation of the hardware. Included in this IP package is a PCI/PCI-X interface with AutoDMA capability, as well as various Mercury designed cores. This IP package includes a local control bus (LCB) interface, a DDR SDRAM interface, a dual-port SRAM interface, a high-speed data link (HSDL) interface for inter-FPGA data flow, plus A/D and D/A interfaces with collection control logic. Sophisticated off-chip interfaces such as DDR and source-synchronous LVDS are also included. The team can develop its own application IP and can gain access to the previous functionality via a local user interface. This allows the end-user to focus on developing application-specific functionality and simplifies the integration of that IP. The team will develop its own unique application IP using standard FPGA development tools such the Xilinx ISE. Then, the team can easily integrate the IP into the board by downloading the end-user images into the field-upgradeable flash memory over a simple memory map PCI/PCI-X interface. The ECV4-2 supports up to 16 MB of flash memory that is used to program both FPGAs, which can be reconfigured from the flash at any time. The flash itself can also be reprogrammed at any time.

For completeness, a few of the manufacturer's details about the receiver are noted below. The ECV4-2-2R130-SL-PMCX front panel has 2 SSMC coax input connectors labeled Analog Channel 1-2. Each analog input is single ended. The input is terminated into 50 Ohms. A zero dB attenuator is standard, but other values can be populated when it is necessary to change the analog input range to a larger value (standard is +5.9dBm equals full scale). After the attenuator, the single-ended input is transformer coupled to the 130 MSPS 16 bit A/D converter. This creates the differential input into the A/D converter, sets the full-scale input to be +5.9dBm, and sets the 1dB bandwidth to be up to 350 MHz. The output of the A/D converter is routed into the User FPGA for digital processing. The local interface is implemented in a Xilinx VirtexTM-4 XC4VLX25 FPGA. A Xilinx core is used for the basic PCI-X interface. A local bus interface and a high speed full-duplex LVDS interface to user FPGA connect the PCI-X core to these data busses for data flow. There are 2 DMA controllers: one for input, and one for output. There are several DMA interrupts that are standard, and are passed to 1 PCI interrupt. The local bus is similar in signaling and protocol to the PCI bus. Lastly, the local bus operates at 50MHz.

3. CONCLUSION

The project is a collaborative effort between university and federal scientists. Assembly and test of the instrument is being accomplished in Atmospheric Radar Research Center (ARRC)'s Radar Innovation Laboratory (RIL) prior to integration into the NWRT. At the appropriate time, scientists from the National Severe Storms Lab (NSSL) will take an active role in the integration of this instrument. In the approaching months, specific test data will be collected and reported. As examples of future projects, a few are mentioned: monopulse tracking & subbeam resolution; sidelobe cancelling for ground clutter mitigation; advanced modeling and forecasting; validation of Observing System Simulation Experiments (OSSEs). The digital data will open to the general research community via an open website.

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