5.14 EVALUATION OF A DIGITAL RECEIVER FOR THE RESEARCH AND DEVELOPMENT WSR-88D

D.S. Zrnic* and A. Zahrai
NOAA/National Severe Storms Laboratory, Norman, OK

1. INTRODUCTION

One of the evolutionary changes considered for the network of the WSR-88D is to replace part of the current analogue receiver with digital circuits. The following three reasons are behind the need for a digital receiver. 1) The present receiver is becoming obsolete. 2) The planed upgrade to a dual polarization mode requires two receivers for which there would be no physical space if the present circuits were retained. 3) There is a novel processing scheme which can reduce the standard errors of estimates by a factor of more than 2 compared to the traditional processing schemes; this scheme requires over sampled signals.

Over the last couple of years the Radar Operation Center (ROC) of the National Weather Service and the National Severe Storms Laboratory (NSSL) have been evaluating available receivers that were integrated into autonomous radar data acquisition hardware. This evaluation indicates that it has become possible to meet the current operational requirement of the WSR-88D. As a next step in the process NSSL has procured a low cost commercial digital receiver and begun test to determine its suitability for inclusion into the research and development WSR-88D. This proof of concept is a first step toward possible inclusion into the operational network. Herein we report the status of this endeavor.

2. HARDWARE

The rapid advance in cellular phone technology makes possible economic replacement of a part of current analogue receivers with the digital counterpart. Two crucial components that have become recently available make it possible to build economical digital receivers. These are fast analogue to digital converters (A/D) and digital down-conversion circuits. The A/Ds digitize the signal at intermediate frequencies (57.14 MHz on the WSR-88D) which is then further filtered and down-converted by special integrated circuits. A useful operation prior to the A/D conversion is anti alias filtering, for which we use a 10 MHz bandwidth (3 dB points) analogue filter centered at the IF frequency.

To achieve a large instantaneous dynamic range (> 90 dB) fast analogue to digital converters with at least 14 bits are required. The sampling frequency should be as high as possible so that the Nyquist interval is very large. In this manner the spurious effects introduced by the digitization are spread over a large frequency band for a given fixed integration time. These spurs are then greatly reduced with digital filters that follow the A/D. Therefore, the power in the spurious components is inversely proportional to the sampling (clock) frequency of the converter (Fig. 1). As of this writing 14 bits A/Ds that operate at up to 80 MHz have become available.

Digital down conversion circuits shift the signal to base band in two steps. First multiplication by a sinusoid and cosinusoid (at intermediate frequency) is made and then the results are filtered to preserve the base band of the inphase I and quadrature phase Q components. The sinusoidal signals are generated digitally in a numerically controlled oscillator (NCO) and hence are perfectly balanced in amplitude and phase. Therefore, the output I and Q components have the following properties
- I,Q are balanced in phase and amplitude (hence there are no image spectral components)
- There is no DC offset inherent in the digitization of analogue I,Qs.

The receiver under test is the Echotech ECDR-GC814G/2 (echotek.com). It is a dual channel with two 14 bit 80 MHz A/Ds and one quad down conversion chip, the Gray GC4016 (graychip.com). This chip is at the hart of the circuit. It consists of four independent digital down converter channels and is specified to operate at rates of up to 90 mega samples per second. Pertinent characteristics for our application are listed next.

The input accepts 14 bit data. Each down converter contains an NCO and a mixer to convert the signal to its two baseband components. This is followed by a 5 stage Cascade Integrate Comb (CIC) filter and two stages of block averaging filters to isolate the desired signal.

The tuning frequency is set according to the formula $FREQ = 2^{32}F/F_{CK}$ where F is the desired tuning frequency and F_{CK} is the clock frequency. A phase offset can be specified if needed.

One stage of the CIC filter is equivalent to a uniformly weighted averaging filter (Hogenauer 1981). Therefore five stages are equivalent to application of a moving average five times. There are no multipliers and, in the filtering process, signals are decimated in time. There is no choice here except for gain and decimation factor between 8 and 4096. (Combining two channels can reduce the effective decimation). Hence, the least decimation, after the CIC filter, is 8. The frequency transfer of the CIC filter (with the decimation of 8) is

$$\{\sin(\pi fT8)/\sin(\pi fT)\}^{10},$$

where T is the sample spacing, $T = 1/F_{CK}$.
After the CIC filter there are two weighted moving average filters (tap filters), one with 21 taps the other

Corresponding author address: D.S. Zrnic, NSSL/NOAA 1313 Halley Cr., Norman, OK 73069;

with 63 taps. Choice of weights is available and each tap filter decimates by an additional factor of two which brings the total to 32.

3. DESIGN CONSIDERATION

To incorporate the digital receiver into the WSR-88D requires the following.

a) Choice and generation of the clock frequency
b) An anti alias filter centered on the intermediate frequency f_{if}
c) Appropriate input conditioning (level) of clock and IF signals
d) Choice of the NCO frequency
e) Choice of filter coefficients for the two filters with taps
f) Interface with the signal processor and control computer
g) Design of a calibration scheme

Some of the design options are discussed next. These are inexorably tied to the specific intermediate frequency of the WSR-88D, f_{if} = 57.5491 MHz and the spacing of range resolution volumes (i.e., the gate spacing). The range gate spacing in the current WSR-88D is 250 m (which is also the pulse depth) and is obtained from a count of 16x6/f_{if}. Therefore to generate easily this sample spacing the clock frequency should be n f_{if} /3, where n is an integer. The highest possible n is 4 which produces the clock (i.e., sampling) frequency $F_{CK} = 4f_{if}/3$ = 76.7321 MHz. This choice aliases the sampled IF signal to f_{if}/3 which also becomes the desired NCO frequency F. We have obtained this F_{CK} by the following divide and mix operations f_{if} /3 + f_{if}. With these choices, timing of the digital receiver and the output of samples are in complete synch with the rest of the radar system. There are other possibilites for the clock frequency but these require re-sampling (available within the chip) to generate the spacing of 250 m.

The digital output signals, after decimation by 32, are at a rate of f_{if}/24, or exactly four per 250 m. The process of decimation is sketched in Fig. 2. Note that the input spacing is at $\Delta_1 = 3/(4\ f_{if})$ and after decimation by 8 the spacing is $\Delta_2 = 3x8/(4f_{if}) = 6/f_{if}$. A 250 m range spacing is comprised of 16 Δ_2. At this point the 21 taps filter is well suited to match the pulse depth, even if all the weights are used, provided these are tapered at the beginning and end.

Decimation reduces the number of sampled per 250 m to eight at the output of the first tap filter. Thus of the 63 weights on the second tap filter no more than 9 taps should be used; the rest should be set to 0 to preserve range resolution. The weights are determined so that the combined frequency response and range weighting function of the three filters (CIC, 21 tap, and 63 tap) meet desired specifications. A natural choice that maximizes the SNR for a given resolution in range is obtained with a matched filter. Because there is control of weights on the tap filters an approximately matched filter can be constructed.

4. DYNAMIC RANGE

The combined operation of sampling and digital filtering increases the instantaneous dynamic range of the receiver. This is because the signal to noise level at output of the digital filter is larger than at the input. Thus, the following definition is appropriate. Dynamic range of the digital receiver is the ratio of signal power after the A/D converter and digital filter to the noise power before the same operations under the following assumptions: the noise power at the input to the A/D converter is set at one or less bits and the signal peak voltage at the input equals to the saturation of the A/D (Zrnic 2000).

For specific filters and input autocorrelation of the noise one can compute the increase in dynamic range over the intrinsic dynamic range of the A/D converter. Moreover, it is relatively simple to measure it by injecting a sinusoidal signal at a directional coupler in the waveguide. For a noise of bandwidth B_n, signal bandwidth B_s, and integration as done here with the CIC and tap filters the increase in dynamic range is (Zrnic 2000)

$$B_n/B_s$$

The noise bandwidth B_n = 10 MHz and is primarily determined by the anti alias filter, whereas the signal bandwidth can be approximated by the reciprocal of pulse width (about 600 kHz). The intrinsic dynamic range of a 14 bit A/D is somewhat larger than 68 dB and therefore the increase is expected to be close to 12 dB which makes the total larger than 90 dB.

An additional increase in the dynamic range is possible because in partial saturation (i.e., saturation that occurs sporadically during the filtering time) of the A/D there are some samples that do not saturate the A/D. The precise increase here depends on the choice of the clock frequency. For example if the choice is such that the harmonics (aliased) of the clipped signal are filtered by the digital receiver then the increase corresponds to the amount by which the fundamental harmonic (aliased f_{if}, here f_{if}/3, Fig. 3) at the output of the filter exceeds the saturation value of the input. Fourier analysis indicates that this could be almost 6 dB.

Aliasing of the IF signal and its harmonics is sketched in Fig. 3, whereby the numbers under the frequency axis indicate the harmonic. 1 indicates the fundamental at f_{if}, 2 corresponds to the aliased 2 f_{if}, and so on. For clarity, only the harmonic numbers of the positive side are shown, the numbers for the negative side are symmetric with respect to zero. Therefore, all the harmonics due to saturation (i.e., only odd ones are present) alias on top of each other (3, 5, 7..) and after digital filtering centered on f_{if}/3 the clipped sinusoid is faithfully reproduced. Therefore, much of additional increase in dynamic range is not realizable; an increase of < 3 dB is at most possible. This can be deduced from the fact that aliased harmonics reconstruct perfectly the shape of the clipped sinusoid. In the limit of full saturation (square wave at the output of the A/D) the signal power is exactly 3 dB larger than a sinusoid of equal peak power.

Our present choice of $F_{CK} = 4\ f_{if}/3$ is constrained by the desire to be perfectly synchronized with range gate spacings and the maximum clock rate for the A/D. A clock at $5f_{if}/3$ would achieve perfect synchronization and would allow increase in dynamic range (by close to 6 dB, Zrnic 2001) because most of the aliased harmonics of f_{if} would be filtered. Actually only some harmonics starting

with 4 f_{if} would be aliased on the fundamental f_{if} (these are 4, 6, 9, 11..., Fig. 3), and of these the even ones are normally not present in a saturating signal and the odd ones start with the ninth and are weak. Thus the increased clock frequency will be implemented as soon as a 100 MHz A/D becomes available.

5. CONCLUSIONS

Design considerations for a digital receiver indicate that the present technology should provide adequate dynamic range and signal purity to be compatible with the existing analogue system on the WSR-88D. Commercial receivers meeting the specifications are available and can be interfaced with a nominal amount of effort. As of this writing a receiver is near delivery and pending test will be reported at the conference.

6. REFERENCES

Hogenauer, E.B., 1981: An economical class of digital filters for decimation and interpolation. *IEEE Transactions on Acoustic, Speech, and Signal Processing,* **ASSP-29,** 155-162.

Zrnic, D.S., 2001: Receiver - Signal Processor, Distinction and Implications for calibration. Paper presented at the Calibration Workshop, 81st AMS annual meeting, Albuquerque, NM.

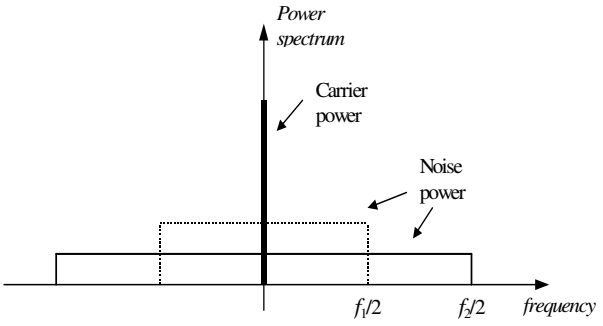

Fig.1. Power spectra of the carrier and noise. The noise spectra are referenced to the peak of the carrier and that is the reason why the noise levels are different. Otherwise for two different sampling frequencies but same integration time the noise would have the same level and the peak of the carrier would be proportional to the number of samples (or sampling frequency).

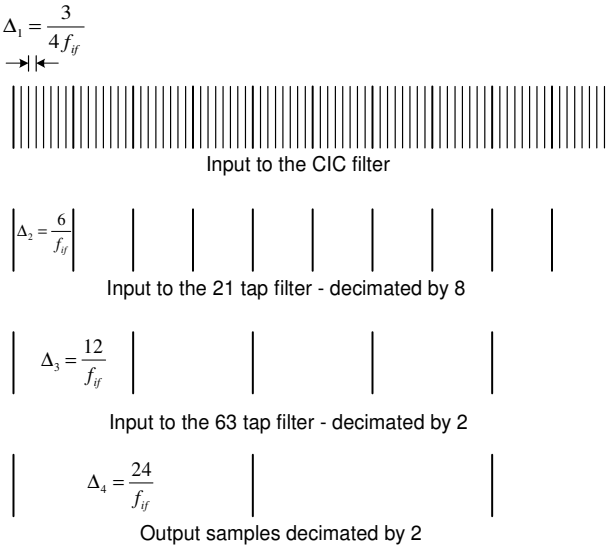

Fig. 2. Depiction of decimation at the various stages of filtering for the choice sampling frequency of $4f_{if}/3$.

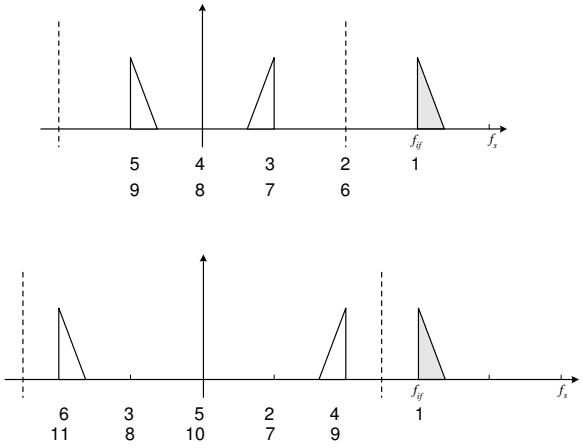

Fig. 3. Spectrum of the IF signal is depicted with a filled triangle; within dashed lines (Nyquist interval) are its aliases due to under sampling. Top graph is for $f_s = 4f_{if}/3$, and the bottom graph is for $f_s = 5f_{if}/3$. Aliased harmonics of the positive part of the IF signal are indicated with numbers (i.e., 2 is aliased $2f_{if}$). Aliased harmonics from the negative part are symmetric with respect to the positive part.