5.10 THE OPEN RADAR DATA ACQUISITION (ORDA) DESIGN FOR THE WSR-88D

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1. INTRODUCTION

Under auspices of the National Weather Service (NWS) and its NEXRAD Product Improvement (NPI) program, the National Severe Storms Laboratory (NSSL) has designed a new architecture for control and signal processing functions in the Radar Data Acquisition (RDA) subsystem of the WSR-88D radar. A prototype based on this new architecture was constructed and has been operating since May of 2000. This prototype was implemented as proof-of-concept for the new design. Therefore, only a subset of critical RDA functions were implemented.

The open-system RDA (ORDA) has been described in various conference papers and reports. This paper presents a highlight of characteristics and features of the new architecture.

2. RDA FUNCTIONS

The RDA is essentially a very large and complex real-time monitoring and control system with extensive signal processing functionality. RDA functions can be listed as:

- Monitor and control antenna
- Monitor and control transmitter
- Monitor and control receiver
- Monitor and control signal processor
- Monitor and control data quality
- Generate base data
- Disseminate base data
- Process user commands

Monitoring and control functions require deterministic processes responding to internal and external events in a timely manner. These type of operations are suitable for a real-time controller and a real-time operating system. Generation of base data is a numerically intensive operation and is best performed by a dedicated digital signal processor.

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Antenna pedestal is controlled by exchanging status and control packets between the pedestal digital control unit (DCU) and a real-time controller. This interface is implemented using a RS-232 serial port. Status and control packets are exchanged every 45 milliseconds. The real-time control software effectively closes the antenna servo loop - it computes and issues new commands from antenna position information during every exchange.

Transmitter and receiver operate from numerous triggers and timing pulses generated by a custom synchronizer module controlled by the real-time controller. The signal processor is synchronized with the receiver by the synchronizer module. Raw data from the receiver is pumped directly into the signal processor to compute reflectivity, velocity, and spectrum width values for each receiver sample.

Data quality is assured by performing several calibration and alignment steps using extensive built-in test circuitry in the receiver. Bulk of base data generation and calibration algorithms are performed by the digital signal processor subsystem controlled by the real-time controller (Torres et. al. 2002).

Data dissemination functions consist of archival of radar data and transmission of these data and status information to users. The users of the RDA area are local and remote maintenance personnel and the associated Radar Product Generator (RPG) operators. Maintenance personnel generally interact with the system in the off-line mode to perform maintenance and troubleshooting functions. The RPG is the primary point of operational control for an entire WSR-88D radar.

3. ORDA ARCHITECTURE

The overall goal of the NPI Program is to gradually upgrade the WSR-88D radar to meet expanding mission needs. The first and prerequisite step is the replacement of obsolete proprietary components with commercial-off-the-shelf (COTS) equipment and software based on open system standards.

Examination of evolutionary requirements in the RDA area alone reveals the need for a highly modular and scalable system. Modularity, scalability and open system standards ensure viability and reduce the impact of obsolescence. Indeed in the new architecture primary emphasis was placed on these features (Zahrai et. al. 1998).

As opposed to the existing RDA where a single processor performs all command, control, and communications functions, in the new design these functions are relegated to specialized subsystems. This functional modularity was achieved by using modern distributed processing techniques and standard networking technology.

Real-time monitoring and control functions are performed by an imbedded real-time node referred to as the RDA signal processing and control (RDASPC). This node basically consists of a single board computer and a timing and synchronization module referred to as the synchronizer. The synchronizer provides complex timing signals and triggers for the transmitter, the receiver, and all built-in test and calibration equipment. The synchronizer also contains interface circuits to convert and condition raw digital values from the receiver and supply these values to the signal processing subsystem.

The RDASPC incorporates a highly scalable multiprocessor signal processing engine with its own high-speed interconnect fabric. A multiprocessor real-time operating system provides UNIX-like function libraries and an application programming interface (API).

A COTS workstation and standard networking equipment perform all non real-time tasks such as user interface, communications, and file system. Utilizing TCP/IP family of protocols allows use of inexpensive networking and communications equipment and provides connectivity benefits previously unavailable. These benefits include remote access and maintenance through the Internet infrastructure.

All computer programs developed during the prototype phase for the real-time controller, the signal processor and the user workstation have been written in C language using a layered client-server architecture.

4. ARCHITECTURE EVOLUTION

Figure 1 shows a simplified block diagram of the RDA signal processing and control subsystem. This configuration represents an evolutionary extension of the original design demonstrating flexibility and scalability of the proposed architecture.

Leveraging recent advances in digital communications technology a COTS multi-channel digital receiver is currently under investigation as a potential replacement for the aging and obsolete analog receiver in the WSR-88D (Zrnic et. al. 2002). Another contributing factor in this beneficial upgrade is that implementation of dual-polarization capability requires two receiver channels for simultaneous reception of horizontal and vertical waveforms. Accomplishment of this task is not possible with the original analog receivers. Initial deployment of the ORDA will not include a digital receiver however.

Figure 1 also shows a Fibre-channel interface used for archival and playback of radar data providing WSR-88D archive level-1 and/or level-2 functionality. Raw digital time-series data from the receiver are referred to as level-1 data and the derived radial data, i.e. reflectivity, velocity, and spectrum width, are referred to as level-2 data. Fibre-channel interface connects the RDASPC subsystem to a high-capacity RAID storage device featuring a 86 Mbytes/sec sustainable data rate. Using this scheme, corrected time-series data are grouped per transmitter pulse, tagged with appropriate header information and are recorded continuously along with derived level-2 data. Over 10 hours of data can be recorded using a typical WSR-88D volume coverage pattern. This capacity can be readily quadrupled using currently available higher capacity disk drives. The storage device is also connected to the ORDA workstation through a secondary Fibre-channel port to allow subsequent perusal and extraction of interesting phenomena without operational disruption. This previously

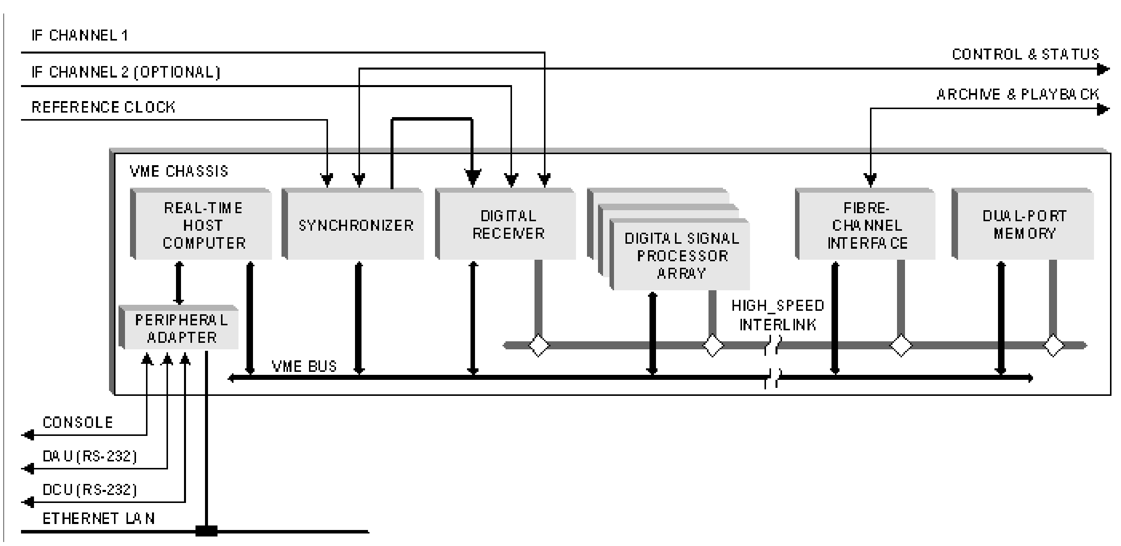

Figure 1: Block Diagram of the RDA real-time subsystem

unavailable capability is now fully functional in the prototype system. However, this capability is not currently required in an operational environment and is primarily intended for research and development.

5. SUMMARY

The overall goal of the ORDA project was to design a highly modular and scalable non-proprietary architecture which would provide all existing functionality and serve as a foundation for all evolutionary enhancements requested by user community. The proposed and partially implemented design achieves these high-level goals by leveraging mainstream industry standards and COTS environments and hardware. All hardware used in this project with the exception of the synchronizer module are commercially available, many from multiple vendors. Operating systems are POSIX compliant and all application programs were developed in C language. The synchronizer module was designed in-house using low cost programmable devices. This module is designed to be a non-repairable item.

6. ACKNOWLEDGMENT

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