P4D.4 DEVELOPMENT OF A DIGITAL IF RADAR TRANSCEIVER SYSTEM

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1. INTRODUCTION

Recent rapid growth in the microelectronics industry has seen the development of high performance analogue-to-digital converters, reconfigurable logic devices and digital signal processors, such that it is possible to quantize down-converted radar signals directly at IF. Using such techniques it is now possible to replace substantial portions of the analogue receiver system with digital signal processing (DSP). In doing so, many of the inherent alignment, maintenance and temperature sensitivity problems can be drastically reduced. In addition to solving many of the traditionally difficult problems associated with analogue receiver systems, a digital system provides an improved linearity, increased linear dynamic range and reduced phase-jitter through reduced AM/PM conversion inherent to IF limiting often used in linear receiver systems.

The key advantages of digital IF processing over equivalent function analogue processing are:

- Zero in-phase and quadrature phase error, gain imbalance and offset (DC bias) errors – which manifest themselves as image spectra or clutter echoes in the Doppler spectra.
- Wider dynamic range with a truly linear response.
- Any number of channels can be constructed with a high degree of repeatability – cross covariance parameters in polarimetric radars are more a function of the target and less a function of the receiver.
- Massively reduced temperature sensitivity.
- Reconfigurable in real-time– For example, the final IF filtering characteristics can be changed on a pulse-to-pulse basis if required.

The remainder of this paper details the hardware developed and the lessons learnt so far.

2. HARDWARE DEVELOPMENT

The ever-increasing performance available from modern signal processing devices paves the way for advanced signal processing functionality to be implemented and operated in real-time. For example, the system developed here is capable of measuring the precise transmitted pulse shape and computing and applying an exact (conjugate) matched filter on a pulse-to-pulse basis.

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Two methods fulfilling the functions required of a digital IF processor have been considered:

- A digital HF transceiver system built by QinetiQ, re-engineered for radar use
- A system built using commercial off the shelf components (COTs)

In both cases the goal was to produce a single PCI card that could be installed into an industry standard rack mounted PC case. Another direct aim was to implement as much of the functionality as software elements so as to allow maximum configurability.

2.1 Adaptation of a digital HF receiver

The QinetiQ software radio receiver is capable of concurrently processing two input signals from +4 dBm full scale to approximately –115 dBm with a DC-30 MHz bandwidth. The input signals a quantized by a pair of 14-bit analogue-to-digital converters (Analog Devices AD6644) The samples are passed to a digital down-converter where the signal is mixed down to provide two baseband signals (I and Q) and the sample rate is decimated to produce a two complex baseband streams. It is the rate of these samples that determine the range-gate sampling interval (although this can be varied by further sample rate interpolation and decimation). The baseband samples are then streamed to an 8 Mb fast static memory on the DSP mezzanine board, which hosts two 32-bit floating-point Analog Devices SHARC signal processors. The DSP processors are interfaced to the host via a standard PCI bus. The whole system is built on a multiplayer printed circuit board that occupies a single PCI slot in a standard PC platform. Figure 1 shows a photograph of the fully populated board showing the layout of the major components.

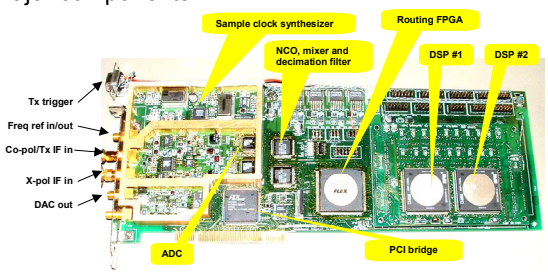

Figure 1: Major components of the QinetiQ derived radar receiver and DSP card.

A number of modifications were made to the base QinetiQ design in order to facilitate its use in radar applications. In order to accommodate higher IF frequencies than 30 MHz, the internal anti-alias input filter was bypassed and replaced by external filters.

The analogue to digital converter although only capable of sampling at a maximum of 65 Msps, has an input bandwidth of 400 MHz. This means that receiver can be used in a band-pass (Shannon) sampling mode with higher IF frequencies. In practice, laboratory tests confirmed satisfactory performance up to 100 MHz, above which the dynamic range quickly degrades. This does however mean that it can be readily adapted to other radar systems with IF frequencies up to 100 MHz using suitable filters. Band-pass sampling places considerable demands on the sample clock. The receiver card employs a carefully designed clock distribution system to minimize clock skew and jitter.

In addition to the IF signals, a number of other signals are required: the transmit fire strobe signal and the polarization strobe (this indicates the radiated polarization; either horizontal or vertical). Additional circuitry was produced to provide a number of optically isolated inputs to poll interrupts on the DSP processors. In order to make coherent measurements two inputs are required: one to measure the receiver IF and another to measure the transmit IF (hence transmit pulse phase). Although this could be done with two dedicated inputs it was found that a fast (<15 ns) GaAs external switching system, with high (>80 dB) isolation provided a satisfactory solution. When the transmit pulse is initiated the input transfer switch is connected to the transmit IF, after a gating period (determined by a precision timer) the input transfer switch is connected to the receiver IF. This still has the advantage of being able to fully sample the transmit pulse (not just to provide a phase estimate) whilst using only one receiver input. This means that it is possible to use the other input for another receiver IF input, i.e. provide a dual channel receiver for polarization diversity. Additionally the complete sampling of the transmit pulse permits the determination of an exact matched filter to maximize signal-to-noise if desired.

2.2 Use of turn-key components

An alternative approach utilising commercially available off the shelf components was also considered. The basis of this system is a digital to analogue converter card based upon the Analog Devices AD6644 (14-bit 65 MSPS) converter (Echotek ECDR-214-PMC) coupled to a signal-processing card using four Analog Devices TigerSHARC processors (Transtech DSP, TS-36N). The block diagram of the ADC card is shown in Figure 2 and that of the DSP card in Figure 3. The major trade-off here is that the hardware is almost too flexible requiring considerable software just to set-up the system. The custom hardware (of section 2.1) on the other hand requires a detailed appreciation of the hardware for even simple software modifications. In both cases the intellectual property is vested largely in the software, since the hardware is based largely on the reference designs of the semiconductor manufacturers.

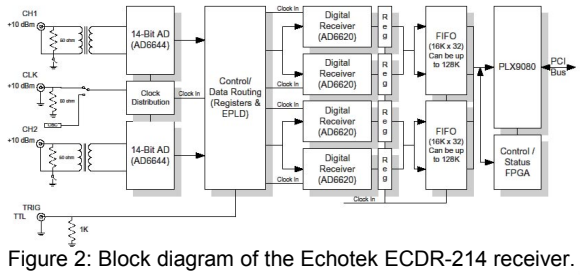

Figure 2: Block diagram of the Echotek ECDR-214 receiver.

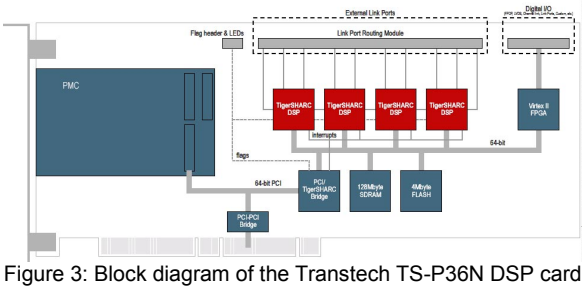

Figure 3: Block diagram of the Transtech TS-P36N DSP card

3. PERFORMANCE EVALUATION

A program of limited tests was undertaken by connecting the QinetiQ derived receiver system in parallel with the S-band CAMRa radar at Chilbolton in the UK. In the absence of precipitation the observation of clutter targets was undertaken. Figure 4 shows the Doppler power spectral density of a clutter target estimated from an FFT of 128 pulses. Reassuringly, it can be seen that the mean Doppler velocity is approximately zero.

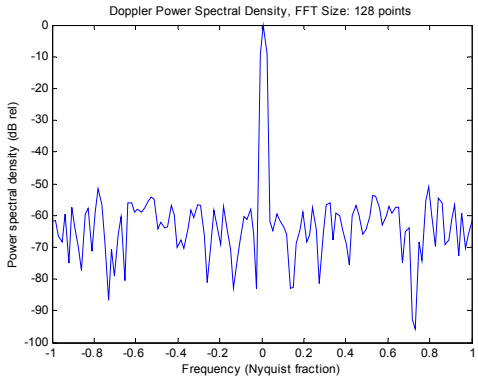

Figure 4: Clutter target Doppler power spectrum derived from FFT of 128 complex I,Q returns.

4. CONCLUSIONS

Two solutions for the implementation of digital IF processing have been presented. Both IF processing systems offer an improvement in performance over conventional analogue receiver systems employing quadrature detection.

5. ACKNOWLEDGEMENTS

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